Fig. 1

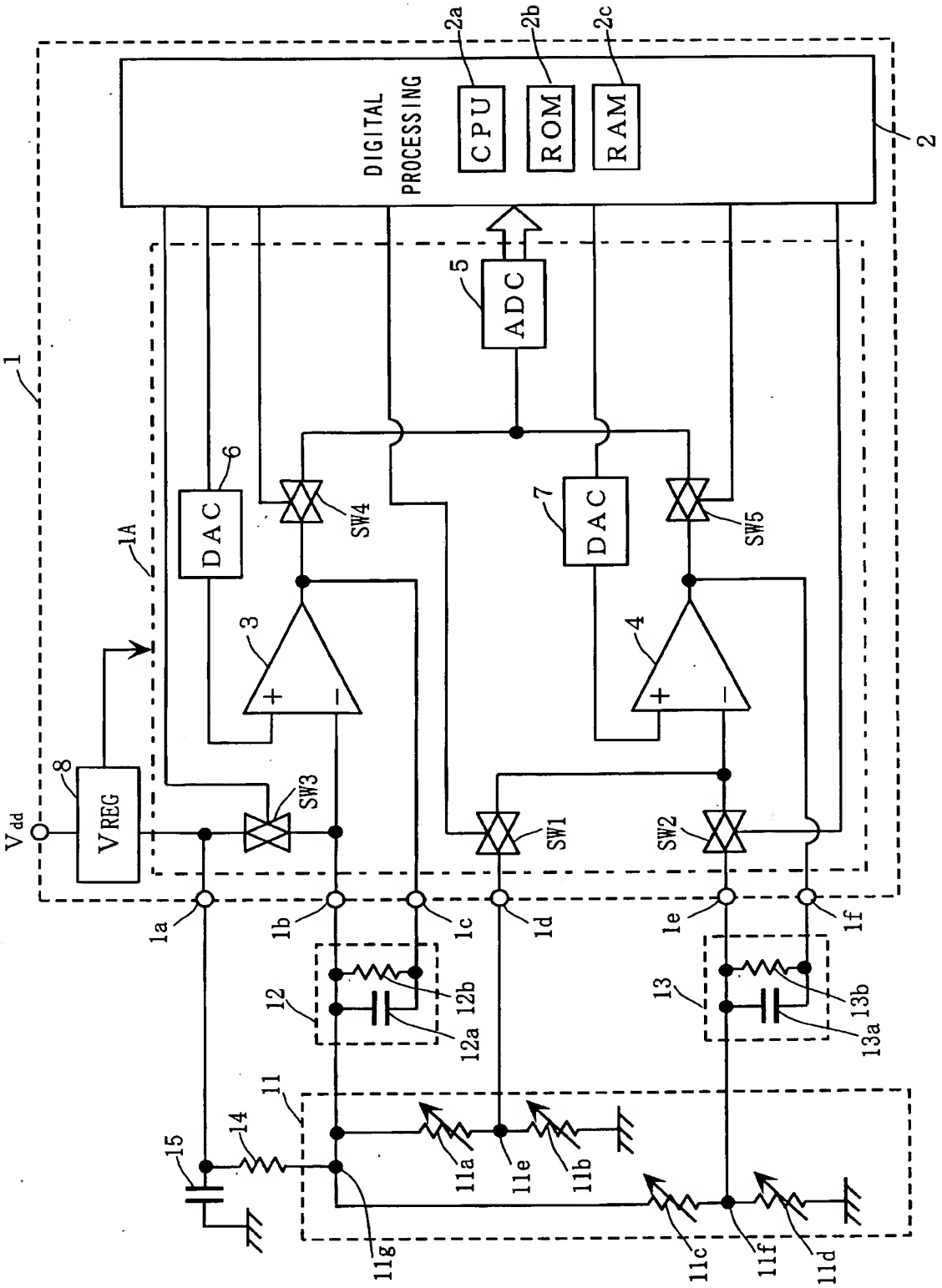

DIGITAL PROCESSING
CPU
ROM
RAM
2a
2b
2c
2
ADC
5
DAC
6
DAC
7
SW4
SW5
SW1
SW2
SW3
VREG
8
Vdd
1
1A
3
4
1a
1b
1c
1d
1e
1f
12
12a
12b
13
13a
13b
11
11a
11e
11b
11g
11c
11f
11d
14
15

Fig. 2

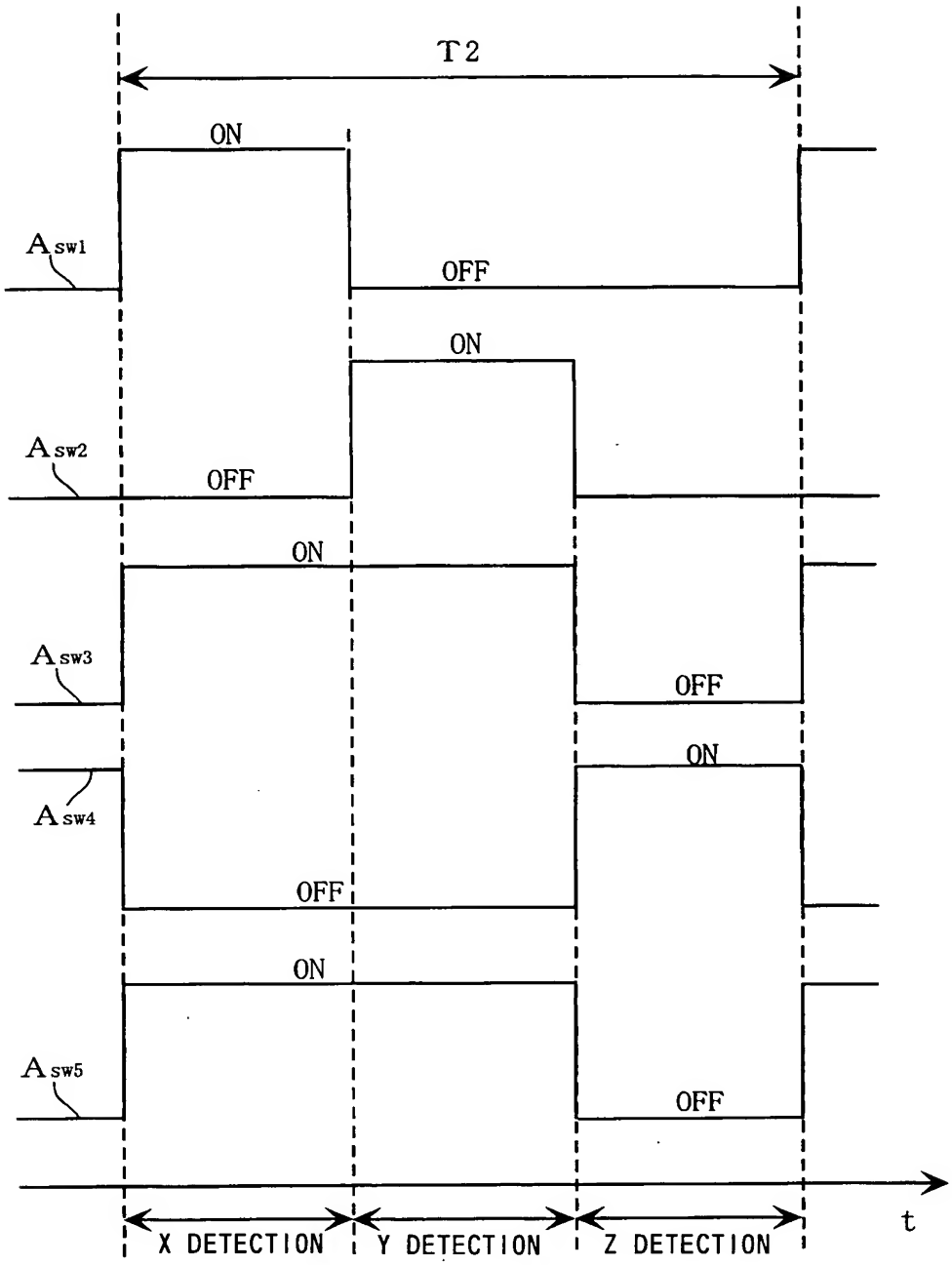

T2
ON
Asw1
OFF
ON
Asw2
OFF
ON
Asw3
OFF
ON
Asw4
OFF
ON
Asw5
OFF
t
X DETECTION
Y DETECTION
Z DETECTION

Fig. 3

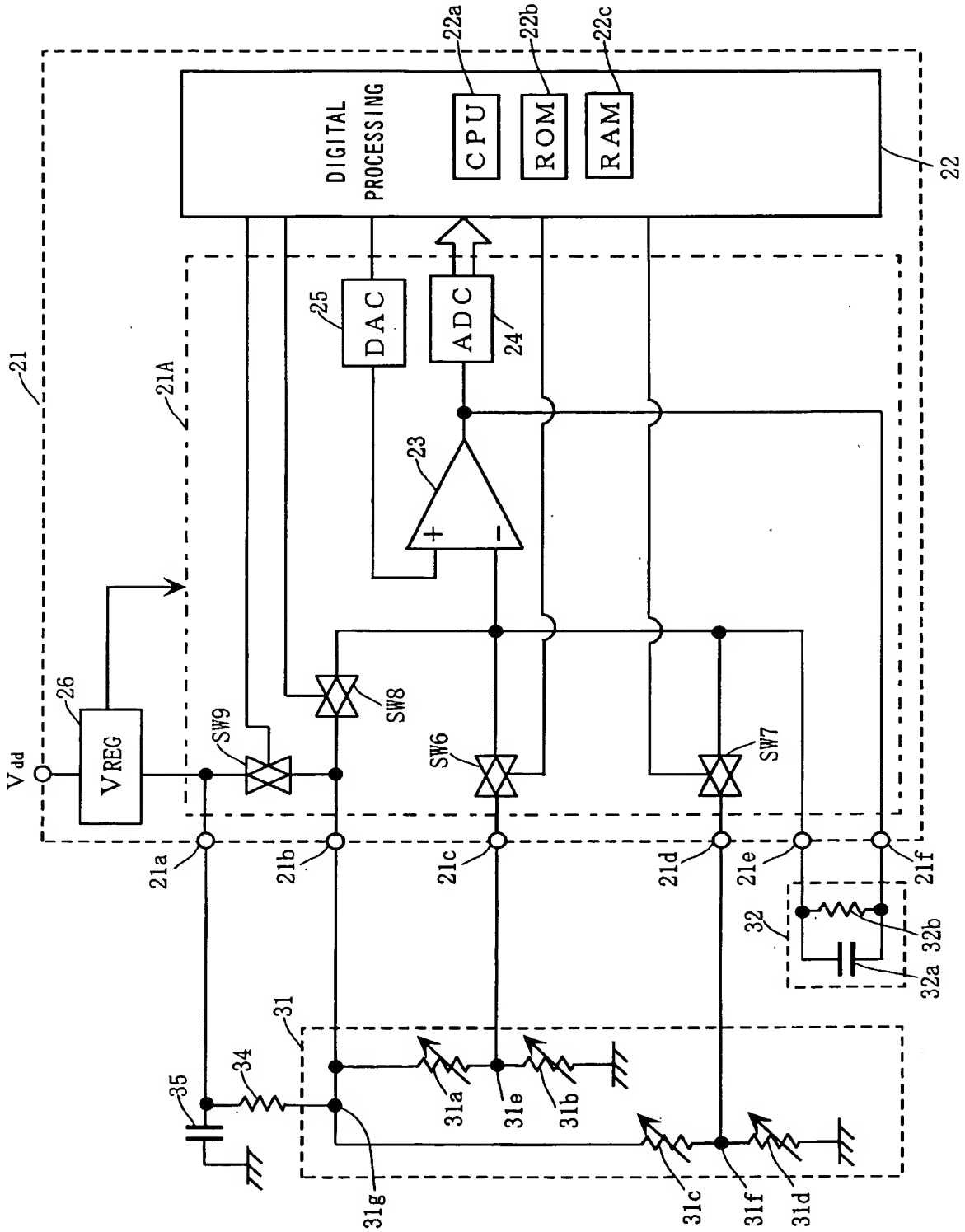

DIGITAL PROCESSING
CPU
ROM
RAM
22
22a
22b
22c
21
21A
DAC
ADC
25
24
23
+
-
26
VREG
Vdd
SW9
SW8
SW6
SW7
21a
21b
21c
21d
21e
21f
32
32b
32a
31
34
35
31a
31e
31b
31g
31c
31f
31d

Fig. 4

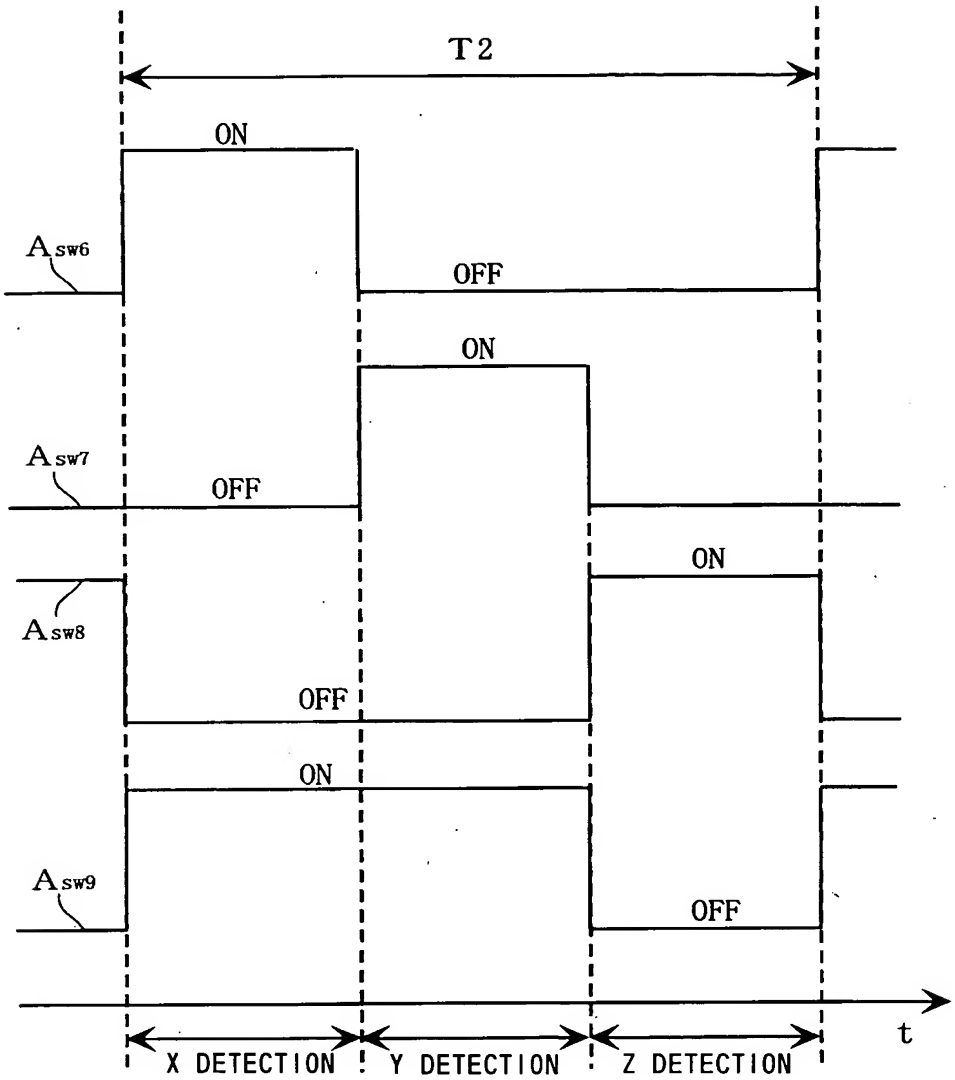

T2
ON
A_{sw6}
OFF
ON
A_{sw7}
OFF
ON
A_{sw8}
OFF
ON
A_{sw9}
OFF
t
X DETECTION
Y DETECTION
Z DETECTION

Fig. 5

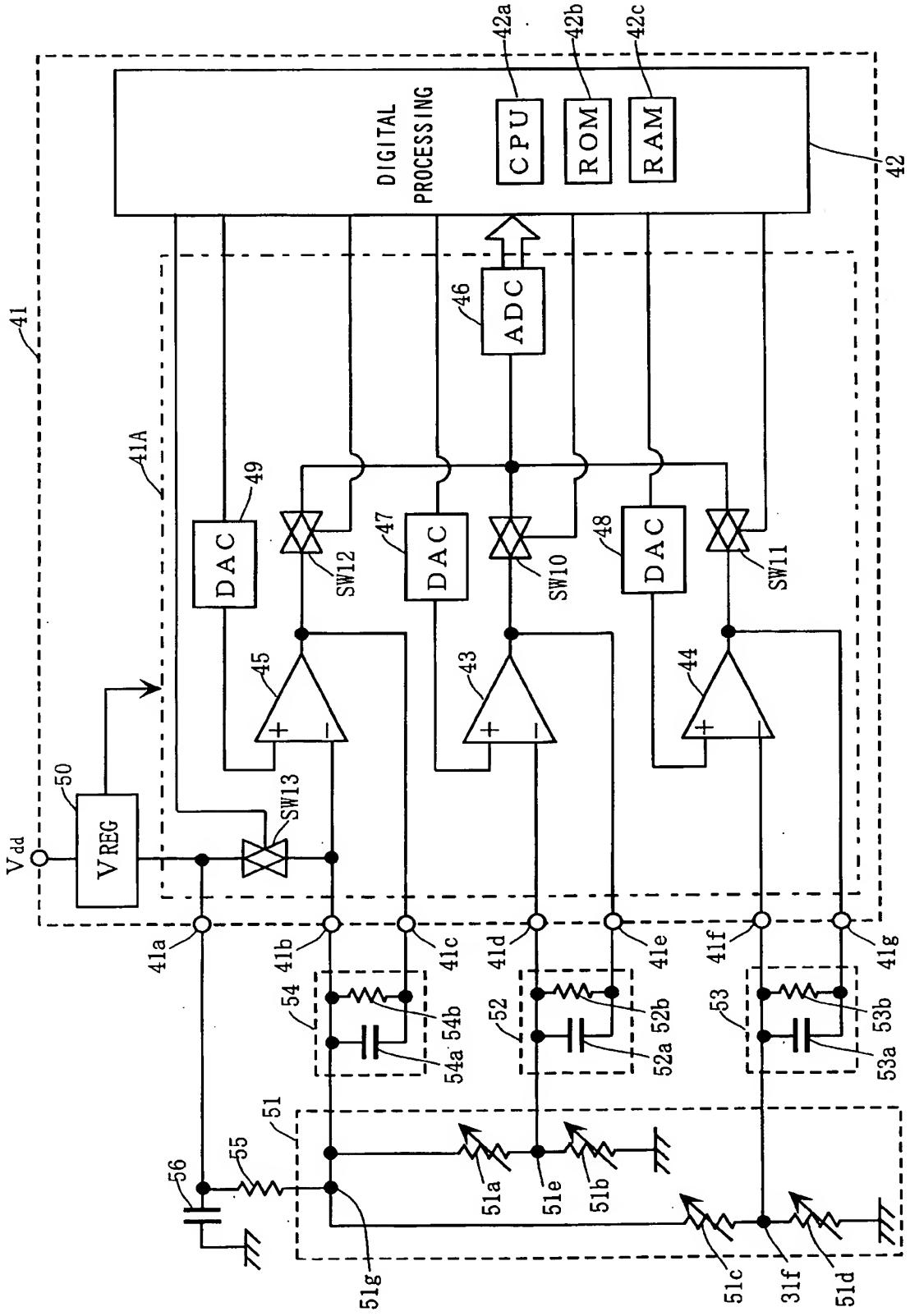

DIGITAL PROCESSING
CPU
ROM
RAM
42
42a
42b
42c
41
41A
ADC
46
DAC
49
47
48
SW12
SW10
SW11
45
43
44
50
VREG
SW13
Vdd
41a
41b
41c
41d
41e
41f
41g
54
54a
54b
52
52a
52b
53
53a
53b
51
51a
51e
51b
51c
31f
51d
51g
55
56

Fig. 6

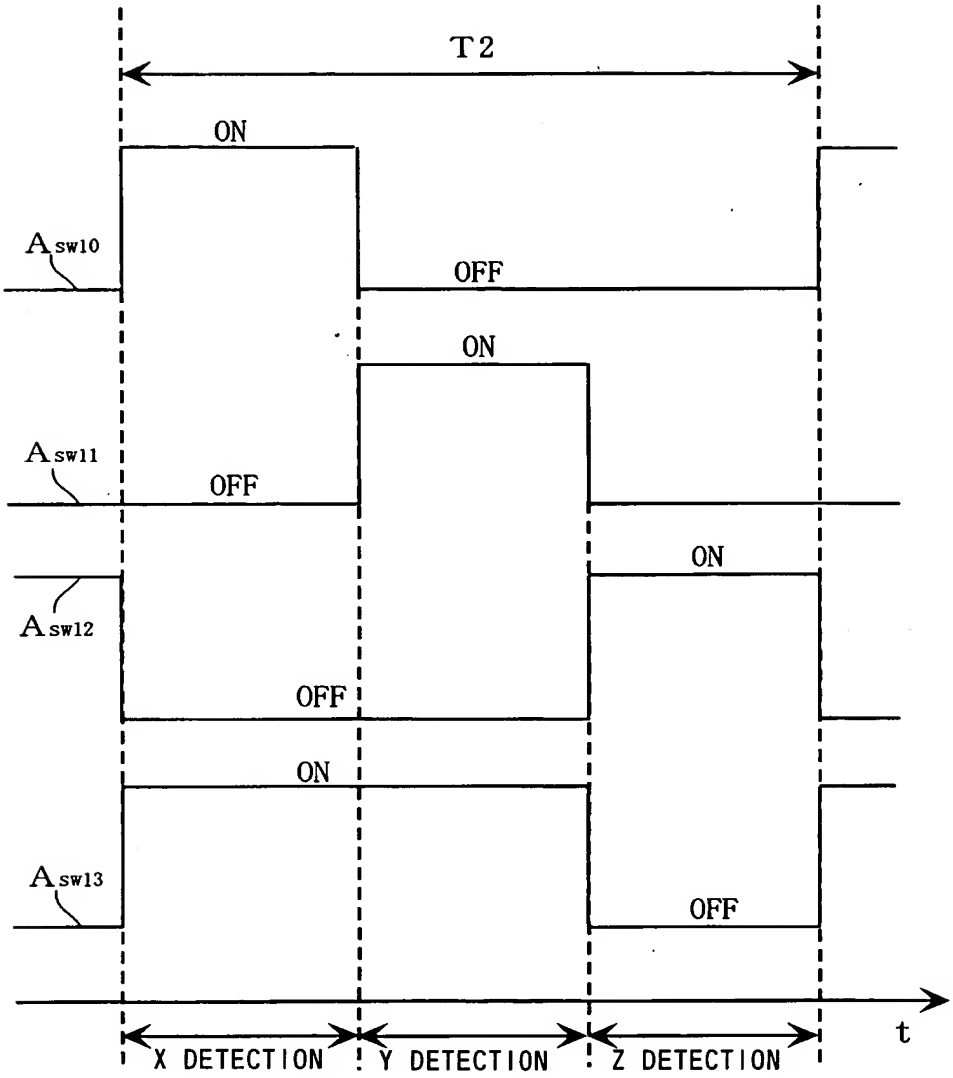

T2
ON
A_{sw10}
OFF
ON
A_{sw11}
OFF
ON
A_{sw12}
OFF
ON
A_{sw13}
OFF
t
X DETECTION
Y DETECTION
Z DETECTION

Fig. 7

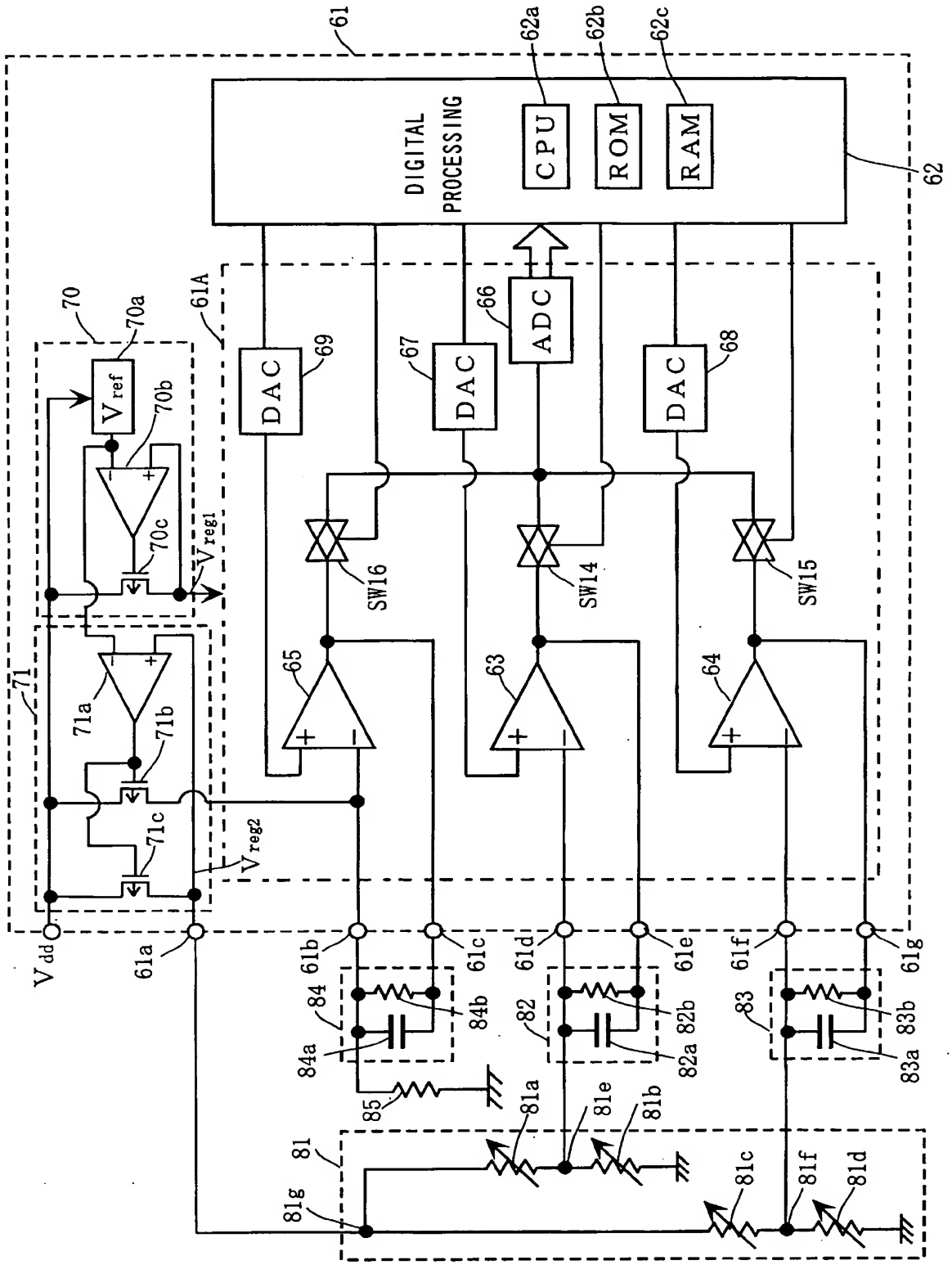

61
62a
62b
62c
DIGITAL PROCESSING
CPU
ROM
RAM
62
61A
70
70a
V ref
70b
70c
V reg1
71
71a
71b
71c
V reg2
V dd
61a
DAC
69
67
DAC
ADC
66
DAC
68
SW16
SW14
SW15
65
63
64
61b
61c
61d
61e
61f
61g
84
84a
84b
82
82a
82b
83
83a
83b
85
81
81a
81e
81b
81c
81f
81d
81g

Fig. 8

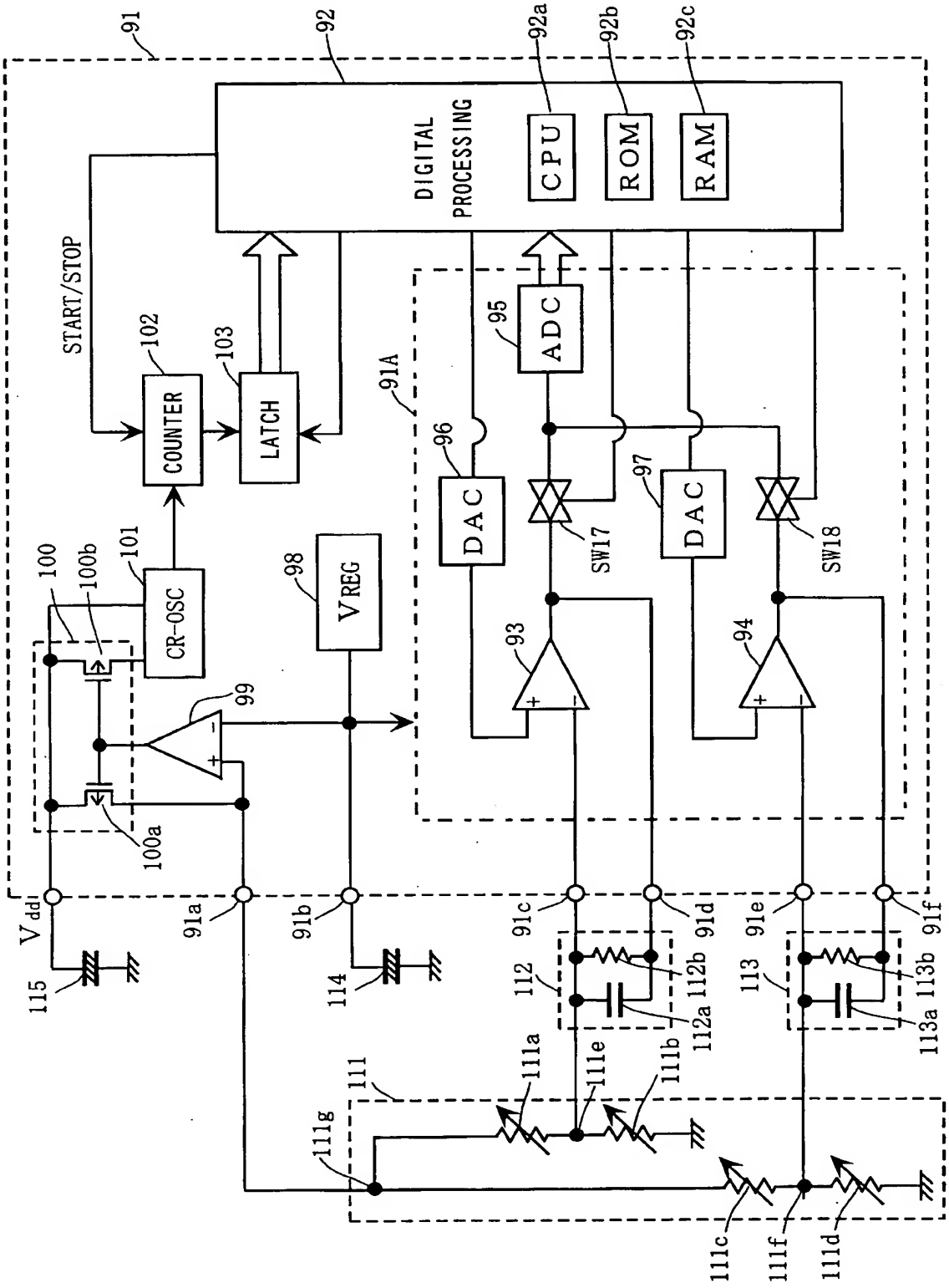
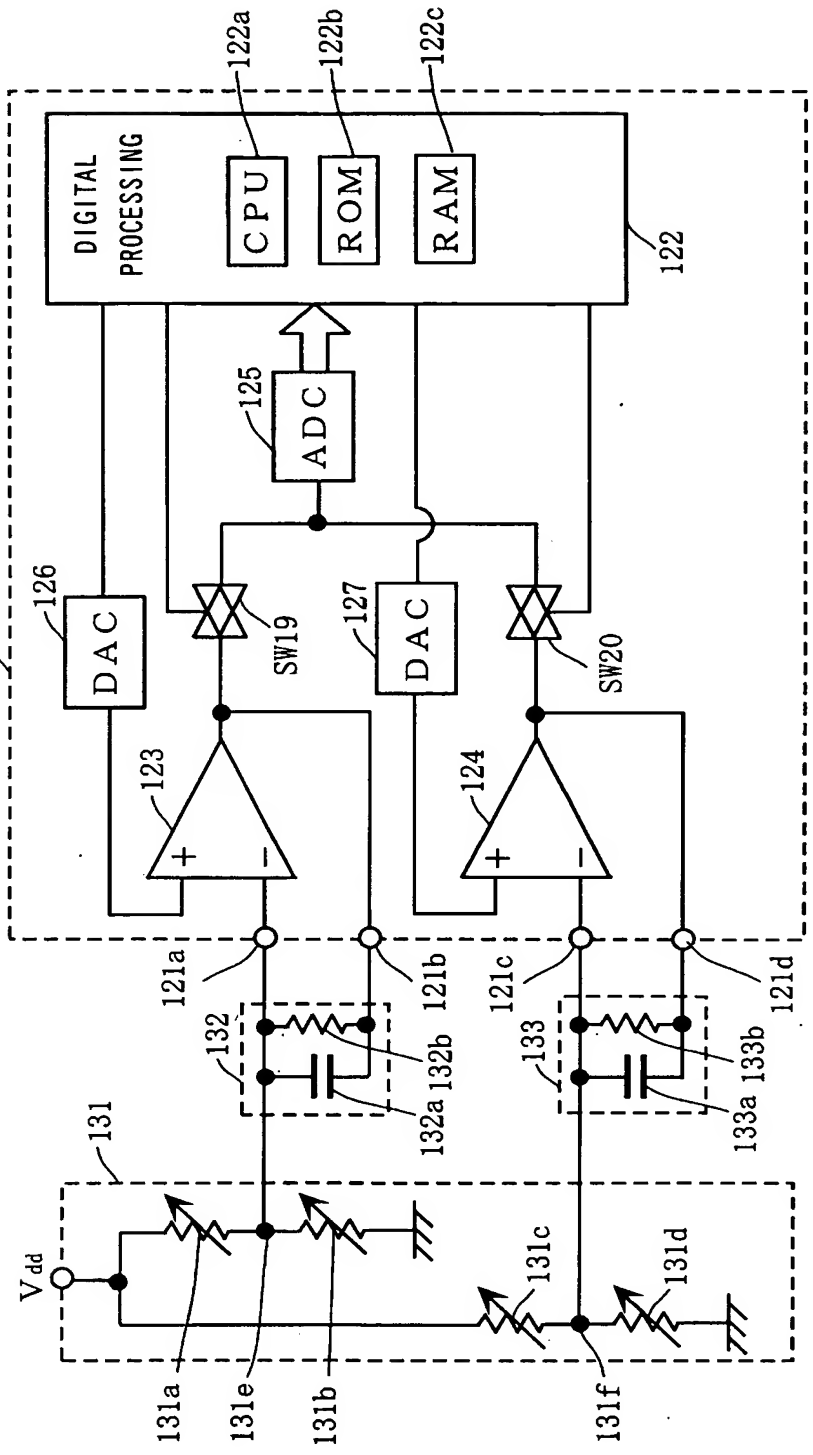
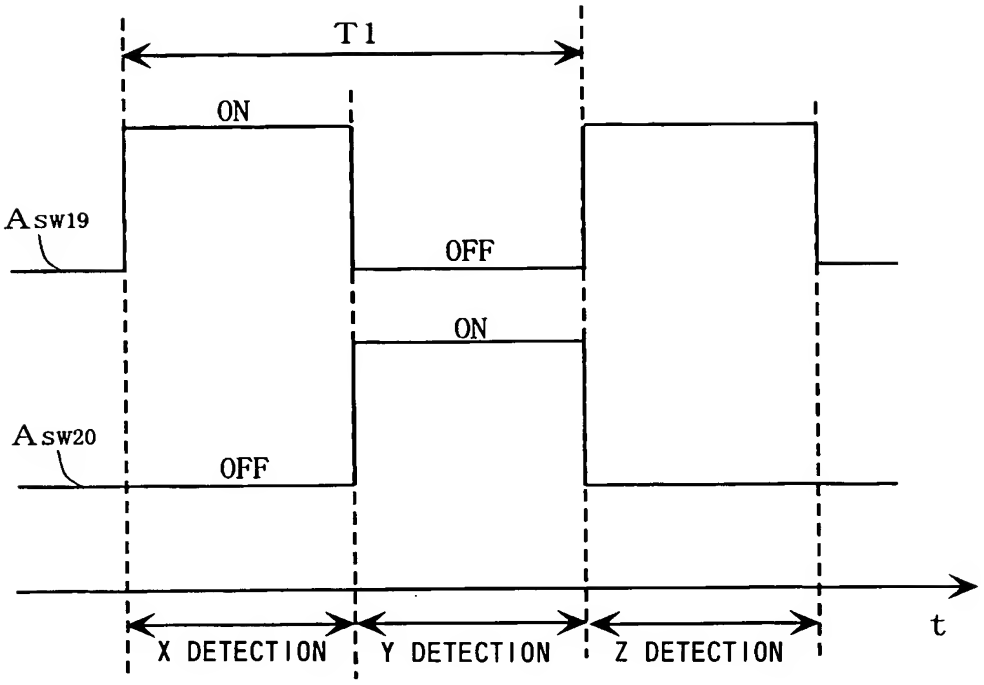

91
92
92a
92b
92c
DIGITAL PROCESSING
CPU
ROM
RAM
START/STOP
102
COUNTER
103
LATCH
91A
95
ADC
96
DAC
97
DAC
SW17
SW18
100
100b
101
CR-OSC
98
VREG
93
94
99
100a
Vdd
91a
91b
91c
91d
91e
91f
115
114
112
112b
112a
113
113b
113a
111
111a
111e
111b
111g
111c
111f
111d

Fig. 9



Prior Art

Fig. 10



Prior Art